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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,335	03/12/2004	Hiromichi Yamada	566,28851CX2	6488

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EXAMINER	
BROOME, SAID A	
ART UNIT	PAPER NUMBER
2628	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/798,335	YAMADA ET AL.	
	Examiner	Art Unit	
	SAID BROOME	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/20/07, 10/14/04, 03/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 14-17 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 10-13. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 2-17 of the currently examined application 10/798,335 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-16 of U.S. Patent 6,727,903. Although the conflicting claims are not identical, they are not patentably distinct from each other because it would have been obvious to one of ordinary skill in the art that the claim language provided in claim 2 of the current application 10/798,335: "*A processor for use with a CPU, a first memory which stores graphics data and a program to be executed by said CPU, and a second memory which stores graphics data…*", though it is a slight variation from claim 1 of U.S. Patent 6,727,903: "*A graphics processing system comprising: a CPU; a first memory which stores graphics data and a program to be executed by said CPU; a second memory which stores graphics data; and a processor…*", it is similar in scope. Therefore though the claims each recite different embodiments, the claimed subject matter of claim 1 in application U.S. Patent 6,727,903 would anticipate analogous storage of graphics data into a first and second memory, as recited in claim 2 of application 10/798,335. Table I listed below is provided to show which claims in the current application 10/798,335 map

to claims of U.S. Patent 6,727,903 on the grounds of nonstatutory obviousness-type double patenting, and Table II is provided below to show which claim limitations from the independent claims 2, 6, 10 and 14 of the current application 10/798,335 map to the independent claims 1, 5, 9 and 13 of U.S. Patent 6,727,903.

TABLE 1

Current Application: 10/798,335	Claims 2-5	6-9	10-13	14-17
U.S. Patent: 6,727,903	Claims 1-4	5-8	9-12	13-16

TABLE II

Current Application: 10/798,335 (Claim 2)	**U.S. Patent: 6,727,903 (Claim 1)**
2. A processor for use with a CPU, a first memory which stores graphics data and a program to be executed by said CPU, and a second memory which stores graphics data and which is separate from said first memory, said processor comprising:	1. A graphics processing system comprising: a CPU; a first memory which stores graphics data and a program to be executed by said CPU; a second memory which stores graphics data; and
a first terminal for outputting an address for reading at least one graphics data stored in said first memory based on a first clock signal; and a second terminal for outputting an address for writing graphics data to said second memory based on a second clock signal,	a processor having a first terminal for outputting an address for reading at least one graphics data stored in said first memory based on a first clock signal and a second terminal for outputting an address for writing graphics data to said second memory based on a second clock signal,
wherein said processor generates graphics	said processor generates an image from

data from said read graphics data, and said first and second clock signals are different from each other.	said read graphics data, and said first and second clocks being clock signals different from each other.
Current Application: 10/798,335 (Claim 6)	**U.S. Patent: 6,727,903 (Claim 5)**
6. A processor for use with a CPU, a first memory which stores graphics data and a program to be executed by said CPU, and a second memory which stores graphics data for displaying and which is separate from said first memory, said processor comprising:	5. A graphics processing system comprising: a CPU; a first memory which stores graphics data and a program to be executed by said CPU; a second memory which stores graphics data for displaying; and
a first terminal; and a second terminal, wherein each terminal outputs an address at a timing different from a timing used to output an address from the other terminal, and	a processor having a first terminal and a second terminal each for outputting an address at a different timing,
wherein said processor reads graphics data from said first memory based on an address output from said first terminal, generates graphics data for displaying from said read graphics data, and writes said graphics data for displaying to said second memory based on an address output from said second terminal.	said processor reads graphics data from said first memory based on an address output from said first terminal, generates graphics data for displaying from said read graphics data, and writes said graphics data for displaying to said second memory based on an address output from said second terminal.

Current Application: 10/798,335 (Claim 10)	**U.S. Patent: 6,727,903 (Claim 9)**
10. A processor for use with a CPU, a first memory which stores graphics data and a program to be executed by said CPU, and a second memory which stores graphics data and which is separate from said first memory, said processor comprising:	9. A graphics processing system comprising: a CPU; a first memory which stores graphics data and a program to be executed by said CPU; a second memory which stores graphics data; and
a first terminal; and a second terminal for outputting addresses,	a processor having a first terminal and a second terminal for outputting addresses,
wherein said processor reads said graphics data from said first memory, generates graphics data from said read graphics data, and writes said graphics data to said second memory, and	said processor reads said graphics data from said first memory, generates graphics data from said read graphics data, and writes said graphics data to said second memory,
wherein said processor outputs addresses from said first terminal to said first memory while at the same time outputting addresses from said second terminal to said second memory.	wherein said processor outputs addresses from said first terminal while outputting addresses from said second terminal.
Current Application: 10/798,335 (Claim 14)	**U.S. Patent: 6,727,903 (Claim 13)**
14. A processor for use with a CPU, a first memory which stores graphics data and a program to be executed by said CPU, a second memory which stores graphics data	13. A graphics processing system comprising: a CPU; a first memory which stores graphics data and a program to be executed by said CPU; a

and which is separate from said first memory, said processor comprising:	second memory which stores graphics data; and
a first terminal; and a second terminal for outputting addresses,	a processor having a first terminal and a second terminal for outputting addresses,
wherein said processor reads said graphics data from said first memory, generates graphics data from said read graphics data, and writes said graphics data to said second memory, and	said processor reads said graphics data from said first memory, generates graphics data from said read graphics data, and writes said graphics data to said second memory,
wherein said processor outputs addresses from said second terminal to said second memory while at the same time outputting addresses from said first terminal to said first memory.	wherein said processor outputs addresses from said second terminal while outputting addresses from said first terminal.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 2-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Tamura (US Patent 4,561,024).

Regarding claim 2, Tamura discloses a processor for use with a CPU (col. 6 lines 42-43: "*The central microprocessor CPU processes the RAM…*", Fig. 1), a first memory which stores graphics data and a program to be executed by said CPU (col. 6 lines 32-43: "*…RAM stores data required in executing the program…and…image data…*" and col. 6 lines 56-57: "*…RAM is transferred to and stored in memory M1…*"), and a second memory which stores graphics data (col. 4 lines 43-44: "*…the second memory M2 includes one scan line of image information…*") and which is separate from said first memory (Fig. 1: M1, M2), said processor comprising:

a first terminal for outputting an address for reading at least one graphics data stored in said first memory based on a first clock signal (col. 3 lines 7-12: "*…image information stored in the first memory M1 is supplied…in synchronism with the clock signal CS11 from the first clock generator CG1, through the first memory control MC1.*", col. 4 lines 43-46: "*…one scan line of image information stored in the first memory M1…is read out by the clock signal from the first clock generator CG1…*", Fig. 1, *in which a first terminal, first memory control ("MC1"), reads graphics (Fig. 1: designated by arrows) from a location stored in the first memory, in which the address of the stored graphics data is accessed in the first memory ("M1") with respect to a first clock signal ("C11")*); and

a second terminal for outputting an address for writing graphics data to said second memory based on a second clock signal (col. 6 lines 58-61: "*…the clock generators…CG2…carry out the magnification of the image data and the magnified image data is stored in the memory M2…*" and col. 4 lines 43-49: "*…the second memory M2 includes one scan line of image information…stored in response to the clock signal*

from the second clock generator CG2...is...magnified...by activating the second memory control MC2…", Fig. 1, *in which a second terminal, second memory control ("MC2", Fig. 1: designated by arrows) enables graphics data to be written to the second memory ("M2") with respect to a second clock signal ("CS22")*),

wherein said processor generates graphics data from said read graphics data, and said first and second clock signals are different from each other (col. 2 lines 46-51: "*…an image digital signal transferred serially in the direction of scan is converted to an analog signal which represents...respective picture cells and it is converted to a second digital signal having a rate different from that of the original or first serial digital signal.*", col. 7 lines 27-28: "*…a second clock signal different from said first clock signal…*", Fig. 1: CS11, CS22).

Regarding claims 3, 7, 11, 15 and 19, Tamura discloses said first memory outputs said graphics data based on said first clock signal (col. 3 lines 7-12: "*…image information stored in the first memory M1 is supplied...in synchronism with the clock signal CS11 from the first clock generator CG1, through the first memory control MC1.*", col. 4 lines 43-46: "*…one scan line of image information stored in the first memory M1...is read out by the clock signal from the first clock generator CG1…*").

Regarding claims 4, 8, 12, 16 and 20, Tamura discloses said second memory outputs said graphics data based on said second clock signal (col. 6 lines 58-61: "*…the clock generators...CG2...carry out the magnification of the image data and the magnified image data is stored in the memory M2…*" and col. 4 lines 43-49: "*…the second memory M2 includes one scan line of image information...stored in response to the clock signal from the second clock generator CG2...is...magnified...by activating the*

second memory control MC2…", Fig. 1, *in which second memory control ("MC2") enables graphics data to be written from a second terminal (Fig. 1: designated by arrows) to the second memory ("M2") with respect to the second clock signal ("CS22")*).

Regarding claims 5, 9, 13, 17 and 21, Tamura discloses wherein said processor, which reads said graphics data from said first memory, generates new graphics data from said read graphics data, and writes said new graphics data to said second memory (col. 6 lines 32-43: "*…The memory ROM stores the program of the process procedures for the image data…The…CPU processes…data in accordance with the program…*", col. 4 lines 43-48: "*…image information stored in the first memory M1 is read out by the clock signal from the first clock generator CG1 and then stored in response to the clock signal from the second clock generator CG2… is…magnified.*" and col. 4 lines 24-25: "*…magnified picture cell data…is stored in...memory M2.*", *in which the processed image graphics data is read from first memory ("M1") is written to second memory ("M2")*).

Regarding claim 6, a processor for use with a CPU (col. 6 lines 42-43: "*The central microprocessor CPU processes the RAM…*", Fig. 1), a first memory which stores graphics data and a program to be executed by said CPU (col. 6 lines 32-43: "*…RAM stores data required in executing the program…and…image data…*" and col. 6 lines 56-57: "*…RAM is transferred to and stored in memory M1…*"), and a second memory which stores graphics data for displaying (col. 4 lines 43-44: "*…the second memory M2 includes one scan line of image information…*") and which is separate from said first memory (Fig. 1: M1, M2), said processor comprising:

a first terminal (Fig. 1, *in which a first terminal, first memory control ("MC1"), reads graphics (Fig. 1: designated by arrows)*); and

a second terminal (Fig. 1, *in which a second terminal, second memory control ("MC2"), reads graphics (Fig. 1: designated by arrows)*),

wherein each terminal outputs an address at a timing different from a timing used to output an address from the other terminal (col. 2 lines 46-51: "*…an image digital signal transferred serially in the direction of scan is converted to an analog signal which represents…respective picture cells and it is converted to a second digital signal having a rate different from that of the original or first serial digital signal.*", col. 7 lines 27-28: "*…a second clock signal different from said first clock signal…*", Fig. 1: CS11, CS22), and

wherein said processor reads graphics data from said first memory based on an address output from said first terminal, generates graphics data for displaying from said read graphics data, and writes said graphics data for displaying to said second memory based on an address output from said second terminal (col. 6 lines 32-43: "*The…CPU processes…data in accordance with the program…*", col. 4 lines 43-48: "*…image information stored in the first memory M1 is read out by the clock signal from the first clock generator CG1 and then stored in response to the clock signal from the second clock generator CG2… is…magnified.*" and col. 4 lines 24-25: "*…magnified picture cell data…is stored in…memory M2.*", *in which the processed image graphics data is read from first memory ("M1") is written to second memory ("M2")*).

Regarding claim 10, Tamura discloses a processor for use with a CPU (col. 6 lines 42-43: "*The central microprocessor CPU processes the RAM…*", Fig. 1), a first memory

which stores graphics data and a program to be executed by said CPU (col. 6 lines 32-43: "*…RAM stores data required in executing the program…and…image data…*" and col. 6 lines 56-57: "*…RAM is transferred to and stored in memory M1…*"), and a second memory which stores graphics data (col. 4 lines 43-44: "*…the second memory M2 includes one scan line of image information…*") and which is separate from said first memory (Fig. 1: M1, M2), said processor comprising:

a first terminal (Fig. 1, *in which first memory control ("MC1") reads graphics through a first terminal (Fig. 1: designated by arrows)*); and

a second terminal for outputting addresses (col. 6 lines 58-61: "*…the clock generators…CG2…carry out the magnification of the image data and the magnified image data is stored in the memory M2…*" and col. 4 lines 43-49: "*…the second memory M2 includes one scan line of image information…stored in response to the clock signal from the second clock generator CG2…is…magnified…by activating the second memory control MC2…*", Fig. 1, *in which second memory control ("MC2") sends graphics through a second terminal (Fig. 1: designated by arrows)*),

wherein said processor reads said graphics data from said first memory, generates graphics data from said read graphics data, and writes said graphics data to said second memory (col. 6 lines 32-43: "*The…CPU processes…data in accordance with the program…*", col. 4 lines 43-48: "*…image information stored in the first memory M1 is read out by the clock signal from the first clock generator CG1 and then stored in response to the clock signal from the second clock generator CG2… is…magnified.*" and col. 4 lines 24-25: "*…magnified picture cell data…is stored in…memory M2.*", *in which*

the processed image graphics data is read from first memory ("M1") is written to second memory ("M2")), and

wherein said processor outputs addresses from said first terminal to said first memory while at the same time outputting addresses from said second terminal to said second memory (col. 3 lines 7-33: "*…image information stored in the first memory M1 is supplied…as a digital signal SD1…in synchronism with the clock signal CS11 from the first clock generator CG1…D/A converter CDA converts the image digital signal SD1 to an analog signal in synchronism with…the first clock generator CG1 and supplies the analog output signal SA to an integrator IL…The integrator IL integrates the signal in synchronism with the clock signal CS21…from the second clock generator CG2 and supplies an integrated output signal SI…in accordance with a ratio of the frequencies of the first and second clock generators…*" and col. 5 lines 42-45: "*…an integrated output signal SI of an analog signal SA…are generated synchronously.*" and is shown in Fig. 4 *in which data output from signal ("SA") that operates at clock signal ("CS12"), is synchronized to output at the same time as signal ("SI") that operates at clock signal ("CS21")*).

Regarding claim 14, Tamura discloses a processor for use with a CPU (col. 6 lines 42-43: "*The central microprocessor CPU processes the RAM…*", Fig. 1), a first memory which stores graphics data and a program to be executed by said CPU (col. 6 lines 32-43: "*…RAM stores data required in executing the program…and…image data…*" and col. 6 lines 56-57: "*…RAM is transferred to and stored in memory M1…*"), a second memory which stores graphics data (col. 4 lines 43-44: "*…the second memory M2 includes one*

scan line of image information…") and which is separate from said first memory (Fig. 1: M1, M2), said processor comprising:

a first terminal (Fig. 1, *in which first memory control ("MC1") reads graphics through a first terminal (Fig. 1: designated by arrows)*); and

a second terminal for outputting addresses (col. 6 lines 58-61: "*…the clock generators…CG2…carry out the magnification of the image data and the magnified image data is stored in the memory M2…*" and col. 4 lines 43-49: "*…the second memory M2 includes one scan line of image information…stored in response to the clock signal from the second clock generator CG2…is…magnified…by activating the second memory control MC2…*", Fig. 1, *in which second memory control ("MC2") sends graphics through a second terminal (Fig. 1: designated by arrows)*),

wherein said processor reads said graphics data from said first memory, generates graphics data from said read graphics data, and writes said graphics data to said second memory (col. 6 lines 32-43: "*The…CPU processes…data in accordance with the program…*", col. 4 lines 43-48: "*…image information stored in the first memory M1 is read out by the clock signal from the first clock generator CG1 and then stored in response to the clock signal from the second clock generator CG2… is…magnified.*" and col. 4 lines 24-25: "*…magnified picture cell data…is stored in…memory M2.*", *in which the processed image graphics data is read from first memory ("M1") is written to second memory ("M2")*), and

wherein said processor outputs addresses from said second terminal to said second memory while at the same time outputting addresses from said first terminal to said first memory (col. 3 lines 7-33: "*…image information stored in the first memory M1*

is supplied...as a digital signal SD1...in synchronism with the clock signal CS11 from the first clock generator CG1...D/A converter CDA converts the image digital signal SD1 to an analog signal in synchronism with...the first clock generator CG1 and supplies the analog output signal SA to an integrator IL...The integrator IL integrates the signal in synchronism with the clock signal CS21...from the second clock generator CG2 and supplies an integrated output signal SI...in accordance with a ratio of the frequencies of the first and second clock generators…" and col. 5 lines 42-45: "*…an integrated output signal SI of an analog signal SA...are generated synchronously.*" and is shown in Fig. 4 *in which data from second memory (Fig. 1: "M2"), which contains a frequency from second clock signal ("CS22",) is output from signal ("SI") that operates at a second clock signal ("CS21"), is synchronized to output at the same time as data from a first memory (Fig. 1: "M1"), which operates at signal ("SA") that operates at a first clock signal ("CS12")*).

Regarding claim 18, a processor for use with a CPU (col. 6 lines 42-43: "*The central microprocessor CPU processes the RAM…*", Fig. 1), a first memory which stores graphics data and program to be executed by said CPU (col. 6 lines 32-43: "*…RAM stores data required in executing the program...and...image data...*" and col. 6 lines 56-57: "*…RAM is transferred to and stored in memory M1…*"), and a second memory which stores graphics data (col. 4 lines 43-44: "*…the second memory M2 includes one scan line of image information…*") and which is separate from said first memory (Fig. 1: M1, M2), said processor comprising:

a first terminal (Fig. 1, *in which first memory control ("MC1") reads graphics through a first terminal (Fig. 1: designated by arrows)*); and

a second terminal for outputting/inputting data (col. 6 lines 58-61: "*…the clock generators…CG2…carry out the magnification of the image data and the magnified image data is stored in the memory M2…*" and col. 4 lines 43-49: "*…the second memory M2 includes one scan line of image information…stored in response to the clock signal from the second clock generator CG2…is…magnified…by activating the second memory control MC2…*", Fig. 1, *in which second memory control ("MC2") can send and receive graphics through a second terminal (Fig. 1: designated by the two-way relationship of the arrows)*),

wherein said processor reads graphics data from said first memory, generates graphics data from said read graphics data, and writes said graphics data to said second memory(col. 6 lines 32-43: "*…the memory ROM stores the program of the process procedures for the image data…The…CPU processes…data in accordance with the program…*", col. 4 lines 43-48: "*…image information stored in the first memory M1 is read out by the clock signal from the first clock generator CG1 and then stored in response to the clock signal from the second clock generator CG2… is…magnified.*" and col. 4 lines 24-25: "*…magnified picture cell data…is stored in...memory M2.*", *in which the processed image graphics data is read from first memory ("M1") is written to second memory ("M2")*),

wherein a transfer amount of data input according to said address output from said first terminal differs from a transfer amount of data output according to said address output from said second terminal (col. 2 lines 46-51: "*…an image digital signal transferred serially in the direction of scan is converted to an analog signal which represents…respective picture cells and it is converted to a second digital signal having*

a rate different from that of the original or first serial digital signal.", col. 7 lines 27-28: "*…a second clock signal different from said first clock signal…*", Fig. 1: CS11, CS22), and

wherein said addresses are output from said first and second terminals to said first and second memories respectively at the same time (col. 3 lines 7-33: "*…image information stored in the first memory M1 is supplied…as a digital signal SD1…in synchronism with the clock signal CS11 from the first clock generator CG1…D/A converter CDA converts the image digital signal SD1 to an analog signal in synchronism with…the first clock generator CG1 and supplies the analog output signal SA to an integrator IL…The integrator IL integrates the signal in synchronism with the clock signal CS21…from the second clock generator CG2 and supplies an integrated output signal SI…in accordance with a ratio of the frequencies of the first and second clock generators…*" and col. 5 lines 42-45: "*…an integrated output signal SI of an analog signal SA…are generated synchronously.*" and is shown in Fig. 4 *in which data from second memory (Fig. 1: "M2"), which contains a frequency from second clock signal ("CS22",) is output from signal ("SI") that operates at a second clock signal ("CS21"), is synchronized to output at the same time as data from a first memory (Fig. 1: "M1"), which operates at signal ("SA") that operates at a first clock signal ("CS12")*).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SAID BROOME whose telephone number is (571)272-2931. The examiner can normally be reached on M-F 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on (571)272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ulka Chauhan/
Supervisory Patent Examiner, Art Unit 2628

/Said Broome/
Examiner, Art Unit 2628